Digital Fundamentals || 3130704 ||
DF || SEM 3 || CHAPTERWISE IMP
Questions

Module - 1 : :Fundamentals of Digital Systems and logic families

1. State and explain De Morgan's theorems with truth tables. OR State and prove DeMorgan Theorem.
2. Discuss Universal gates. Obtain AND, OR , NOT , EX-OR gate using NAND and NOR gates.
3. Perform the Given subtraction using 2's complement method.
4. Explain Excess-3 code and Gray Code.
5. Express the Boolean function F = AB + A'C in a product of maxterm.
6. Give comparison of TTL and CMOS family. OR Compare TTL, ECL, & CMOS logic families
7. Convert 1000 0110 (BCD) to decimal, binary & octal.
8. Minimize the logic function X = A(B' + C')(A + D) . Also realize the reduced
function using NOR gates only.9. List out problems of asynchronous circuits. Also exemplify any two
problems with suitable examples.
10. List out various logic families. Also list the characteristics of digital ICs.
11. Implement the following function with NAND and NOR Gate. F(a,b,c) = Σ (0,6)
12. Discuss the advantages and disadvantages of TTL Logic Family.
13. Obtain canonical Sum of Product form of following function: F=AB+ACD.

Module - 2 : Combinational Digital Circuits

1. Reduce the expression in SOP and POS form using K-map. F(A,B,C,D) = ∑m (1,5,6,12,13,14) + d(2,4)
2. Explain briefly 3 to 8 line decoders.
3. What is a multiplexer? The logic circuit and function table explain the working of 4 to 1 line multiplexer.
4. Draw 1) logic circuit of 4:1 MUX (2) logic diagram of 3-line to 8-line decoder (3) logic circuit of Full Adder and Full Subtractor with truth table. (4) logic circuit of 2x4 Decoder (5) logic circuit for 2-Bit Magnitude Comparator
5. Realize the expression Y(A, B, C, D) = Σ m(15, 7, 4, 6, 8, 9, 12, 14) using an 8:1 MUX.
6. Design (1) 1-Bit Full Adder using 3x8 Decoder. (2) full adder and realization full adder using 3X8 Decoder and 2 OR gates.
7. Solve the following Boolean functions by using K-Map. Implement the

simplified function by using logic gates F = (w,x,y,z) = Σ (0,1,4,5,6,8,9,10,12,13,14)
8. With a neat block diagram explain the function of the encoder. Explain priority encoder?
9. Implement the following Boolean functions with a multiplexer and Decoder. F(w, x, y, z) = Σ (2, 3, 5, 6, 11, 14, 15)
10. Design a combinational logic circuit whose output is high only when the majority of inputs (A, B, C, D) are low.
11. How to generate 8x1 MUX using 4x1 MUX.
12. Implement the following function using 8X1 MUX F (A, B, C, D) = Σ m (0, 1, 3, 4, 8, 9, 15)

Module - 3 : Sequential circuits and systems

1. What is the race condition in JK flip-flop?
2. Design (1) 1 - bit Magnitude Comparator. (2) 4-bit ripple counter using negative edge triggered JK flip flop. (3) Counter to generate the repetitive sequence 0, 3, 5, 7, 4 using D FFs. (4) 3-bit ripple up-counter using negative edge triggered JK flip flops. Also draw the waveforms. (5) 3-bit binary counter. (6) synchronous counter for sequence: 0→1→3→4→5→7→0 using T flip-flop. (7) 4-bit Ring counter using D flip-flop OR Design JK flip-flop using D flip-flip.
3. Give the comparison between synchronous and asynchronous counters.
4. Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.
5. Distinguish between combinational and sequential logic circuits.
6. Explain the output glitch problem generated due to different switching speed of the FFs. Also explain state assignment to eliminate glitches with the help of suitable example & necessary diagrams.
7. How many FFs are required to design FSM with 100 states? Give calculation
8. Explain Serial Transfer w.r.t Shift Register with suitable example.
9. Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.
10 Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T – flip-flops.

Module - 4 : A/D and D/A Converters

1. Describe magnitude comparator.
2. Derive and draw logic circuit for BCD to Excess-3 Code converter.
3. Explain the specification of D/A converter.
4. Explain R-2R ladder type D/A converter
5. Explain Successive Approximation type A/D converter.

Module - 5 : Semiconductor memories and Programmable logic devices

1. Compare ROM, PLA and PAL
2. Using 8x4 ROM, realize the expressions F1 = AB'C + ABC' + A'BC, F2 = A'B'C + A'BC' + AB'C', F3 = A'B'C' + ABC. Show the contents of all locations.
3. List down the various types of ROMs and discuss two of them.
4. Write a short note on Programmable Logic Arrays.5. Explain classification of Memories.
6. Explain the types of ROM.